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EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/614,817	LEE, CHEOL-HO	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/9/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement filed 09 July 2003 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because of the following reasons:

Document number 10-33051 (Korea - 3/16/02) is not present in Applicant's file.

The remaining cited foreign patent documents (AE through AL as listed on the PTO-1449) are present in the application; however an English translation of the abstract for these seven documents was not provided to the Examiner.

The two cited U.S Patent documents have been fully considered by the Examiner.

The information disclosure statement has been placed in the application file, but all the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Drawings

3. The drawings filed on 09 July 2003 are deemed acceptable.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Computer system comprising a plurality of memory buses operating in multi-channel mode and control method thereof".

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Applicant failed to disclose the "computer readable storage" as described in claims 14-16 in written description of the specification. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-18 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claims 1, 6, 14 and 20, one of ordinary skill in the art would be unable to determine how the claimed "read memory information" can be compared if only one of the "at least one of a plurality of memory modules" is read. The read memory information could not in fact be compared with anything if it itself is the only information read. The Examiner will further treat these claims on their merits based on the assumption that Applicant intended to compare the read memory information of "at least two memory modules selected from the plurality of memory modules".

Claims 2-5, 7-13 and 15-18 further limit one of the rejected base claims, therefore they too are rejected as failing to comply with the enablement requirement.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 6-9, 14, 16-17 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Wirt (US Patent 6,003,121).

As for claim 6, Wirt teaches a computer having a plurality of memory buses operating in a multi-channel mode, comprising:

a controller (Fig. 2, element 210) determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory information of at least one of a plurality of memory modules, connected to the respective memory buses, to each other (characteristics of each memory module can be either read from an EEPROM, or the memory module itself (as claimed by applicant) – col. 2, lines 15-19 - Wirt's system can determine if the memory modules are operating on one or more channel, and group them based on their characteristics by comparing the characteristic information extracted from the memory – col. 3, lines 47-57); and

an output unit providing information whether the plurality of memory buses operate in the multi-channel mode according to the determination by the controller (information regarding the configuration of the system is tracked via a system of counters (group, channel, and device) – col. 3, lines 59-67. The counters are incremented as information regarding the configuration, based on the configuration data stored in the modules, is received. The counters act as a means of outputting information regarding the channeling mode of the system – col. 4, lines 10-23). More specifically, the channel counter is the unit that outputs the configuration (single or multiple channels depending on the count).

As for claim 7, Wirt teaches the computer according to claim 6, wherein the memory information of the memory modules connected to the respective memory buses comprises serial presence detect (SPD) data stored in the respective memory modules (col. 3, lines 1-8 – the read data includes serial presence detect data. Note

though the teachings include reading the SPD data from the EEPROM, Wirt teaches an embodiment wherein no EEPROM is present, hence the SPD is read from directly from the modules (col. 2, lines 15-19)).

As for claim 8, Wirt teaches the computer according to claim 7, wherein the SPD data comprises memory capacity information of the respective memory modules (Wirt teaches memory size as one of the characteristics of his system (col. 2, lines 4-10)).

As for claim 9, Wirt teaches the computer according to 6, wherein the controller examines an existence of an arrangement of the memory modules connected to the plurality of the memory buses that allows the plurality of the memory buses to operate in the multi-channel mode, when the controller determines that the plurality of the memory buses do not operate in the multi-channel mode (col. 3, lines 18-35 – once the memory characteristics have been read, a determination can be made whether or not a group is full (i.e. has four members). Additional groupings can then be made based on adding additional groupings based on similar characteristics of the modules, hence adding additional channels. With the addition of these groupings Wirt's system can add channels (for example, adding a channel when operating in single channel mode will now enable the system to operate in multi-channel mode).

As for claim 14, Wirt teaches a computer readable storage controlling a computer according to a stored process of:

reading memory information of at least one of a plurality of channeled memory modules connected to respective memory buses (Fig. 2, depicts an

memory controller (element 210) which is connected to a plurality of memory modules (element 110). Characteristics of each memory module can be either read from an EEPROM, or the memory module itself (as claimed by applicant) – col. 2, lines 15-19);

comparing the read memory information to each other (Wirt's system can determine if the memory modules are operating on one or more channel, and group them based on their characteristics – col. 3, lines 47-57); and

outputting multi-channel mode information of the memory buses based upon the comparing (information regarding the configuration of the system is tracked via a system of counters (group, channel, and device) – col. 3, lines 59-67. The counters are incremented as information regarding the configuration, based on the configuration data stored in the modules, is received. The counters act as a means of outputting information regarding the channeling mode of the system – col. 4, lines 10-23).

As for claim 16, Wirt teaches the computer readable storage of claim 14, wherein the comparing comprises comparing memory capacities of the channeled memory modules to each other to determine if same memory capacity memory modules are separately connected to each memory bus, respectively (again referring to col. 3, lines 47-57, the BIOS code determines the characteristics of a memory device by reading it, then groups the memories according to similar characteristics (i.e. size (col. 2, lines 7-10)). By doing so, Wirt's system is able to determine if the memory capacities of each bus are either the same or different).

As for claim 17, Wirt teaches the computer of claim 6, further comprising:

a BIOS ROM performing a power on self test (POST) during booting of the computer (Wirt's system aims at grouping the memory devices during boot-up when POST occurs (col. 1, lines 6-8). Further Wirt teaches the BIOS code making its determination of and reading of memory characteristics during boot-up (i.e. during the system's POST) – col. 1, lines 25-32), and wherein the controller is software stored in the BIOS ROM and determining the multi-channel mode memory bus operation during the POST (in one embodiment, the BIOS code (program) uses the information stored in the controller's DRD register to make the determination step as claimed by applicant – col. 2, lines 50-57. See also col. 2, lines 30-38).

As for claim 19, Wirt teaches a method, comprising:

outputting multi-channel mode memory bus information based upon memory information of channeled memory modules (just as explained under the rejection of claim 4, information regarding the configuration of the system is tracked via a system of counters (group, channel, and device) – col. 3, lines 59-67. The counters are incremented as information regarding the configuration, based on the configuration data stored in the modules, is received. The counters act as a means of outputting information regarding the channeling mode of the system – col. 4, lines 10-23).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-13, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wirt in further view of Michelet et al. (hereinafter Michelet) US Patent 6,845,277 B1.

As for claim 1, Wirt teaches a method of controlling a computer having a plurality of memory buses operating according to a multi-channel mode, comprising:

reading memory information of at least one of a plurality of memory modules connected to the respective memory buses (Fig. 2, depicts an memory controller (element 210) which is connected to a plurality of memory modules (element 110). Characteristics of each memory module can be either read from an EEPROM, or the memory module itself (as claimed by applicant) – col. 2, lines 15-19).

Wirt further teaches determining whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information with each other (Wirt's system can determine if the memory modules are operating on one or more channel, and group them based on their characteristics – col. 3, lines 47-57).

Though Wirt teaches determining and outputting whether the memory buses operating in multi-channel mode, he does not teach displaying it.

Michelet however teaches a hardware monitoring process having on screen display capability which displays and reports information back to the user including the system's memory configuration and hardware features during the booting process (col. 6, lines 49-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Wirt to further include Michelet's hardware monitoring process. By doing so, Wirt's system would (in addition to determining the channel mode) be able to display the channel mode configuration (and other hardware information pertinent to the memory) to the user. This combination would provide Wirt with a hardware monitoring system, which is critical for maintenance and hardware failure prevention (as taught by Michelet – col. 1, lines 13-17).

As for claim 2, Wirt teaches the method of claim 1, wherein the read memory information comprises serial presence detect (SPD) data stored in the respective memory modules (col. 3, lines 1-8 – the read data includes serial presence detect data. Note though the teachings include reading the SPD data from the EEPROM, Wirt teaches an embodiment wherein no EEPROM is present, hence the SPD is read from directly from the modules (col. 2, lines 15-19)).

As for claim 3, Wirt teaches the method of claim 2, wherein the SPD data comprises memory capacity information of the respective memory modules (Wirt teaches memory capacity as one of the characteristics of his system (col. 2, lines 4-10)).

As for claim 4, Wirt teaches the method of claim 1, further comprising examining an existence of an arrangement of the memory modules connected to the plurality of the memory buses that allows the plurality of the memory buses to operate in the multi-channel mode, when the comparing determines that the plurality of the memory buses do not operate in the multi-channel mode (col. 3, lines 18-35 – once the

memory characteristics have been read, a determination can be made whether or not a group is full (i.e. has four members). Additional groupings can then be made based on adding additional groupings based on similar characteristics of the modules, hence adding additional channels. With the addition of these groupings Wirt's system can add channels).

As for claim 5, though Wirt teaches determining and outputting whether the memory buses operating in multi-channel mode, he does not teach displaying it.

Michelet however teaches a hardware monitoring process having on screen display capability which displays and reports information back to the user including the system's memory configuration and hardware features during the booting process (col. 6, lines 49-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Wirt to further include Michelet's hardware monitoring process. By doing so, Wirt's system would (in addition to determining the channel mode) be able to display the channel mode configuration (and other hardware information pertinent to the memory) to the user. This combination would provide Wirt with a hardware monitoring system, which is critical for maintenance and hardware failure prevention (as taught by Michelet – col. 1, lines 13-17).

As for claim 6, Wirt teaches a computer having a plurality of memory buses operating in a multi-channel mode, comprising:

a controller (Fig. 2, element 210) determining whether the plurality of the memory buses operate in the multi-channel mode by comparing memory

information of at least one of a plurality of memory modules, connected to the respective memory buses, to each other (characteristics of each memory module can be either read from an EEPROM, or the memory module itself (as claimed by applicant) – col. 2, lines 15-19).

Wirt further teaches determining whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information with each other (Wirt's system can determine if the memory modules are operating on one or more channel, and group them based on their characteristics – col. 3, lines 47-57). Though Wirt teaches determining and outputting whether the memory buses operating in multi-channel mode (outputting via the channel counter unit), he does not teach visually outputting which is later claimed in the dependant claim 10. Though claim 6 is rejected under 35 USC § 102(b) as stated above, Wirt in further view of Michelet teaches the concept of visually outputting the information.

Michelet teaches a hardware monitoring process having on screen display capability which displays and reports information back to the user including the system's memory configuration and hardware features during the booting process (col. 6, lines 49-55).

As for claim 7, Wirt teaches the computer according to claim 6, wherein the memory information of the memory modules connected to the respective memory buses comprises serial presence detect (SPD) data stored in the respective memory modules (col. 3, lines 1-8 – the read data includes serial presence detect data. Note though the teachings include reading the SPD data from the EEPROM, Wirt teaches

an embodiment wherein no EEPROM is present, hence the SPD is read from directly from the modules (col. 2, lines 15-19)).

As for claim 8, Wirt teaches the computer according to claim 7, wherein the SPD data comprises memory capacity information of the respective memory modules (Wirt teaches memory size as one of the characteristics of his system (col. 2, lines 4-10)).

As for claim 9, Wirt teaches the computer according to 6, wherein the controller examines an existence of an arrangement of the memory modules connected to the plurality of the memory buses that allows the plurality of the memory buses to operate in the multi-channel mode, when the controller determines that the plurality of the memory buses do not operate in the multi-channel mode (col. 3, lines 18-35 – once the memory characteristics have been read, a determination can be made whether or not a group is full (i.e. has four members). Additional groupings can then be made based on adding additional groupings based on similar characteristics of the modules, hence adding additional channels. With the addition of these groupings Wirt's system can add multiple channels).

As for claim 10, though Wirt teaches determining and outputting whether the memory buses operating in multi-channel mode, however he fails to teach outputting it in visual form.

Michelet however teaches a hardware monitoring process having on screen display capability which displays and reports information back to the user including the

system's memory configuration and hardware features during the booting process (col. 6, lines 49-55) – See claim 6 above.

As for claim 11, the computer according to claim 10, wherein the controller is a determining program determining whether the plurality of the memory buses operate in the multi-channel mode (in one embodiment, the BIOS code (program) uses the information stored in the controller's DRD register to make the determination step as claimed by applicant – col. 2, lines 50-57. See also col. 2, lines 30-38).

As for claim 12, Wirt teaches the computer according to claim 11, wherein the determining program is stored in a BIOS ROM (col. 2, lines 26-35 – the BIOS code is stored in an EEPROM memory).

As for claim 13, though Michelet teaches an output unit comprising a monitor to display information about the hardware/memory arrangement (col. 4, lines 55-60).

As for claim 17, Wirt teaches the computer of claim 6, further comprising:

a BIOS ROM performing a power on self test (POST) during booting of the computer (Wirt's system aims at grouping the memory devices during boot-up (col. 1, lines 6-8). Further Wirt teaches the BIOS code making its determination of and reading of memory characteristics during boot-up (i.e. during the system's POST) – col. 1, lines 25-32), and wherein the controller is software stored in the BIOS ROM and determining the multi-channel mode memory bus operation during the POST (in one embodiment, the BIOS code (program) uses the information stored

in the controller's DRD register to make the determination step as claimed by applicant – col. 2, lines 50-57. See also col. 2, lines 30-38).

As for claim 20, Wirt teaches a method of determining a multi-channel mode memory bus operation of a computer having a plurality of memory buses connected to corresponding channeled memory modules, the method comprising:

executing a program to determine the multi-channel mode memory bus operation during a power on self test, the program controlling the computer according to a process of (in one embodiment, the BIOS code (program) is executed during system start up (i.e. POST), and it uses the information stored in the controller's DRD register to make the determination step as claimed by applicant – col. 2, lines 50-57. See also col. 2, lines 30-38):

reading memory information of at least one of the channeled memory modules connected to the memory buses respectively (Fig. 2, depicts an memory controller (element 210) which is connected to a plurality of memory modules (element 110). Characteristics of each memory module can be either read from an EEPROM, or the memory module itself (as claimed by applicant) – col. 2, lines 15-19);

comparing the read memory information to each other (Wirt further teaches determining whether the plurality of the memory buses operate in the multi-channel mode by comparing the read memory information with each other (Wirt's system can determine if the memory modules are operating on one or more channel, and group them based on their characteristics – col. 3, lines 47-57));

Though Wirt teaches determining and outputting whether the memory buses operating in multi-channel mode, he does not teach displaying it.

Michelet however teaches a hardware monitoring process having on screen display capability which displays and reports information back to the user including the system's memory configuration and hardware features during the booting process (col. 6, lines 49-55).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Wirt to further include Michelet's hardware monitoring process. By doing so, Wirt's system would (in addition to determining the channel mode) be able to display the channel mode configuration (and other hardware information pertinent to the memory) to the user. This combination would provide Wirt with a hardware monitoring system, which is critical for maintenance and hardware failure prevention (as taught by Michelet – col. 1, lines 13-17).

9. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wirt in further view of Kawamata (US Patent 6,535,420 B1).

As for claim 15, Wirt teaches he computer readable storage of claim 14, wherein the memory information comprises, device structure (page size) and logical bank information (number of banks), type information (number of row and column bits) and capacity information (memory size) – col. 2, lines 4-10.

Wirt however fails to teach storing manufacturer information along with the other data listed above.

Kawamata however teaches an electronically rewritable non-volatile semiconductor memory device which is capable of storing the memory manufacture's information in a hidden block of memory (col. 1, lines 40-47).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Wirt to use Kawamata's system of storing critical information (such as manufacturer's information) in the hidden memory. By doing so, Wirt would have a means of storing this information in a protected area to prevent it from being overwritten (Kawamata - col. 1, lines 40-47).

10. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wirt in further view of Cepulis et al. (hereinafter Cepulis) US Patent 6,496,945 B2.

As for claim 18, Wirt fails to include a north bridge in his system, however Cepulis teaches a computer system implementing fault detection and isolation using unique ID codes which utilizes a north bridge (Fig. 1, element 106) which is used to interface between the master controller (140) and a plurality of memory modules (112) – col. 5, lines 43-53 and col. 6, lines 17-19. The master controller controls the north bridge, which in turn controls the memory modules during the POST operation (col. 6, lines 53-67). .

It would have been obvious to one of ordinary skill in the art at the time of the invention for Wirt to further include Cepulis's system of implementing fault detection and isolation. By doing so, Wirt would not only benefit by having a system of detecting and isolating device failures which is critical to most computer systems (as taught by Cepulis in col. 1, lines 33-49), but also Wirt would then be able to more efficiently track failed

devices without the need for running time consuming utility programs (Cepulis - col. 4, lines 13-23).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Stevens et al. (US Patent 6,636,957 B2) teaches a method and apparatus for configuring and initializing a memory device and a memory channel.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

REGINALD G. BRAGDON
PRIMARY EXAMINER